a semiconductor chip mounted on the die pad and having a main electrode and a subelectrode smaller in area than the main electrode;

A1 cont.

two inner leads configured to connect the main electrode and the subelectrode on the semiconductor chip to corresponding connecting pads of the plurality of external leads, respectively, the two inner leads each having a portion of a cut remainder of a tie bar.

A2

11. (Amended) The semiconductor device according to claim 8, wherein the tie bar comprises a plurality of sub tie bars connecting between the two inner leads and arranged separately.

12. (Amended) The semiconductor device according to claim 8, wherein the die pad has a notch in a portion that faces a longitudinal side of the tie bar.

A3

15. (Amended) A semiconductor device comprising:

a plurality of external leads;

a first and a second die pad placed side by side adjacent to the plurality of external leads;

a first and a second semiconductor chip each having a main electrode and a subelectrode smaller in area than the main electrode;

two pairs of inner leads configured to connect the main electrode and the subelectrode on each of the first and the second semiconductor chip to corresponding connecting pads of the plurality of external leads, respectively, each pair of the inner leads having a portion of a cut remainder of a tie bar;

a protruding lead portion formed vertically on one side of the first die pad which faces the second die pad; and

a connecting lead portion formed integrally with one of the inner leads which is connected to the main electrode on the second semiconductor chip mounted on the second die

A3 pad and having a notch engaged with the protruding lead portion so that the connecting lead portion and the protruded lead portion are electrically joined together.

20. (Amended) The semiconductor device according to claim 15, wherein the die pad has a notch in a portion that faces a longitudinal side of the tie bar. A4

Please add new Claims 21-26 as follows:

? 21. (New) A semiconductor device comprising: Diode ; highlighted.

A5 a transistor chip having a first main electrode and a gate electrode on an upper surface of the transistor chip, a second main electrode on a bottom surface of the transistor chip, and a Schottkey diode formed between the first and the second main electrodes in the transistor chip;

S-electrode D. electrode

(1) Next to FET according to patents. (2) clm 17 → 11 to MOSFET (3) Fig 8 = same to Davis

Sub B1

a package base to which the second main electrode of the transistor chip is joined and connected;

an inner lead frame made of a sheet metal, a first end of the inner lead frame being connected to the main electrode to cover at least a part of the Schottky diode, a second end of the inner lead frame being connected to a package lead. Ext. lead

w, cu alloy (8) (new matter)

22. (New) The semiconductor device according to claim 21, wherein the first end of the inner lead frame covers the Schottky diode entirely.

23. (New) The semiconductor device according to claim 21, wherein the transistor chip includes an N-channel MOSFET.

Sub B2 1b3

24. (New) A semiconductor device comprising:

a transistor chip having a first main electrode and a gate electrode on an upper surface of the transistor chip, a second main electrode on a bottom surface of the transistor chip, a transistor region including a transistor, operation of the transistor being controlled by the first

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